EC1834 201.1

Seite 1 / 201.1

TODMA RESET RESETDRV TC VA0 XA0 AEN BHE CLK DACK0BRD DACK0 DACK1 DACK2 DACK3 DMACS DMAAEN INTA INTRCS1 INTRCS2 IOR IOW GTI LOCK MASTER MEMADRSEL MEMCS16 MEMR MEMW NMIADRCS NMIREGCS PPICS RESETDRV S0 S1 S2 TIMERCS XIOR XIOW XMEMR XMEMW YIOR YIOW

SPW2
SPW1
PS1+5
XI[0..15]
XA[0..19] VA0 BHE
DI[0..15]
XA[0..19]

File: EC1834_201.1.kicad_sch

EC1834_201.3 RAM

Seite 3 – RAM

(MEMR MEMW MDPOE MDPEE)
MD[0..15]
(MEM[0..7] WE RAS0 RAS1 CAS1 CAS0)

File: EC1834_201.3.kicad_sch

R52 – KWH 3936.
Widerstandsarray mit gemeinsamen
Pin 8 getauscht gegen RN mit gemeinsamen Pin 1!

EC1834 201.2

Seite 2 / 201.2

Y RDYTODMA RESET RESETDRV TC VA0 XA0 AEN BHE CLK DACK0BRD DACK0 DACK1 DACK2 DACK3 DMACS DMAAEN INTA INTRCS1 INTRCS2 IOR IOW GTI LOCK MASTER MEMADRSEL MEMCS16 MEMR MEMW NMIADRCS NMIREGCS PPICS RESETDRV S0 S1 S2 TIMERCS XIOR XIOW XMEMR XMEMW YIOR YIOW

SPW1
MD[0..15]
(MEM[0..8] RAS0 RAS1 CAS1 CAS0 WE)
SPW2

File: EC1834_201.2.kicad_sch

Power

Seite 4
Stromversorgung

SPW1
SPW2

File: Power.kicad_sch

Bus

DI[0..15]

(XD AEN AENBRD AENBROW AENDMA ALE BHE BS-/WAIT CLK CLK86 DACK0 DEN DT-/R DRQ0 DRQ1 DRQ2 DRQ3 HOLDA HRQDMA IED INT IOCHRDY IORW IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ8 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15 MASTER MDPEE MDPOE MEMR NPNPI NMI PB3 PCLK OSC OSC1 QS0 QS1 ROY

A[0..19] VA0 BHE)

Seite 5 – BUS

File: Bus.kicad_sch

Mario Göbel 2022
Sheet: /
File: EC1834-Board.kicad_sch
Title: EC1834 Hauptplatine
Size: A1 | Date: 2022-09-12 | **Rev: 1**
KiCad E.D.A. kicad (6.0.7) | Id: 1/6

X1 Bus Connector auf Seite "BUS"

WDx = Drahtbrücken

Durch WD3 deaktiviert

Durch WD2 deaktiviert

offen! WD3

WD2

WD1 offen!

L in CPU Zyklus T3 oder RDY LOW

L wenn kein Speicherzugriff

H wenn kein Speicherzugriff

H Pullup R10

Bei der Verwend. d. K1810GF84 entfällt E1

D5 p11 Koord C1 / Blatt 201.2

D64A PIN Pos abweichend von Zeichnung 1.13.120030.0/04

DMA Page Register Steuerung

Mario Göbel 2022
Sheet: /EC1834 201.1/
File: EC1834_201.1.kicad_sch

Title: EC1834 Hauptplatine 201.

Size: A2	Date: 2022-09-12	Rev:
KiCad E.D.A. kicad (6.0.7)		Id: 2/6

BIOS FC000-FFFFF

BIOS FC000-FFFFF

BIOS Erweiterung F8000-FBFFF

BIOS Erweiterung F8000-FBFFF

NMI Maskierung
via Port A0h
80h NMI erlaubt
00h NMI verboten

Parity Behandlung

NMI Maskierung

entfällt auf 1834M!

entfällt auf 1834M!

Mario Göggel 2022
Sheet: /EC1834 201.2/
File: EC1834_201.2.kicad_sch

Title: EC1834 Hauptplatine 201.2

Size: A2	Date: 2022-09-12	Rev: 1
KiCad E.D.A. kicad (6.0.7)		Id: 3/6

MD[0..15]

{MEM[0..7] WE RAS0 RAS1 CASL CASH}

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD8 — U2164 D81A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD8 — U2164 D99A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD0 — U2164 D110A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD0 — U2164 D125A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD9 — U2164 D80A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD9 — U2164 D98A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD1 — U2164 D109A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD1 — U2164 D124A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD10 — U2164 D79A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD10 — U2164 D97A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD2 — U2164 D108A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD2 — U2164 D123A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD11 — U2164 D78A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD11 — U2164 D96A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD3 — U2164 D107A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD3 — U2164 D122A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD12 — U2164 D77A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD12 — U2164 D95A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD4 — U2164 D106A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD4 — U2164 D121A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD13 — U2164 D76A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD13 — U2164 D94A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD5 — U2164 D105A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD5 — U2164 D120A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD14 — U2164 D75A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD14 — U2164 D93A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD6 — U2164 D104A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD6 — U2164 D119A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD15 — U2164 D74A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 → MD15 — U2164 D92A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD7 — U2164 D103A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 → MD7 — U2164 D118A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASH → A0–A7, WE, RAS, CAS, DI; 14 — U2164 D73A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASH → A0–A7, WE, RAS, CAS, DI; 14 — U2164 D91A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS0 CASL → A0–A7, WE, RAS, CAS, DI; 14 — U2164 D102A

MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 WE RAS1 CASL → A0–A7, WE, RAS, CAS, DI; 14 — U2164 D117A

MD1 1
MD2 2
MD0 3
MD10 4
MD3 5
MD6 6
MD11 7
MD4 8
MD7 9
MDPEE 10
MD12 11
MD5 12
MD13 13
MDPOA 14
MD15 15
MEM5 16
MEM7 17
MD14 18
MEM0 19
MEM3 20
MEM4 21
MEM6 22
MEM1 23
MEM2 24
MDPEA 25
MDPOE 26
MD9 27
MD8 28
PS5
PS5

MDPOA

MDPOE

W5 1

Br3

KR531LI1 10 9 D90C 8 &

MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 → D0–D8; F 5; N 6 — KR 531 IP5 D114A

MDPEA

MDPEE

Br2

W4 1

KR531LI1 5 4 D90B 6 &

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 → D0–D8; F 5; N 6 — KR 531 IP5 D113A

{MEMR MEMR MDPOE MDPEE}

MEMR

MDPOE

MDPEE

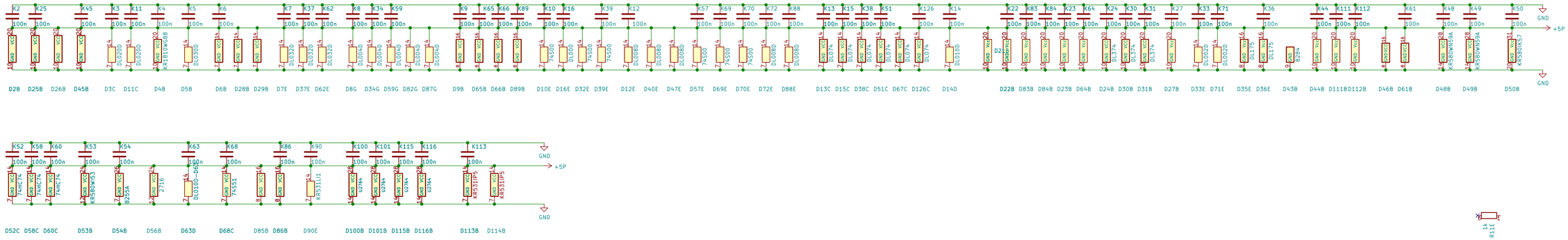
MEMR DL004D MEMR
5 1 6
D87C

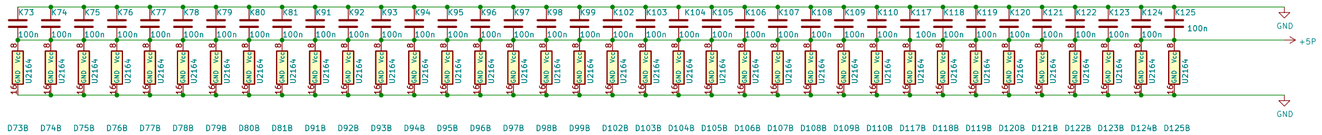
Mario Gögel 2022

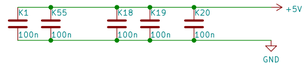
Sheet: /EC1834_201.3 RAM/
File: EC1834_201.3.kicad_sch

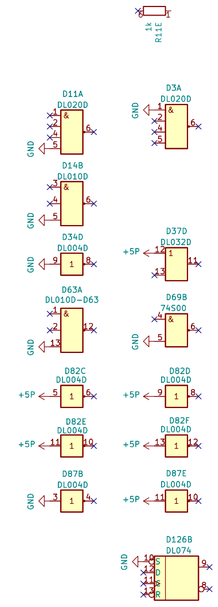
Title: EC1834 Hauptplatine 201.2–RAM

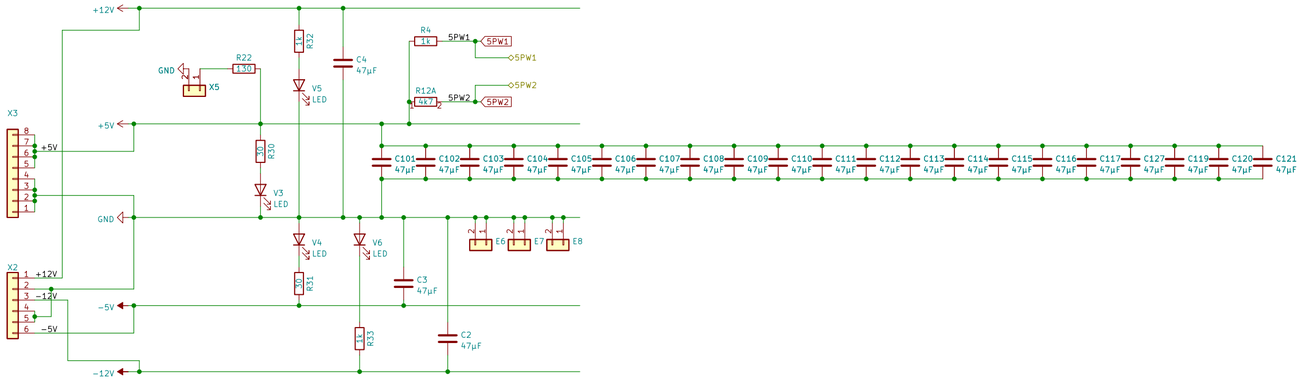
Size: A3	Date: 2022-09-12	Rev: 1
KiCad E.D.A. kicad (6.0.7)		Id: 4/6











Mario Göbel 2022
Sheet: /Power/
File: Power.kicad_sch

Title: EC1834 Hauptplatine 201.2–Power

Size: A2	Date: 2022-09-12	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 5/6

D[0..15]
{A[0..19] VA0 BHE}

X1.2 X1.4 X1.6 X1.8 X1.1 X1.3 X1.5 X1.7

GND RESET +5V IRQ2 −5V DRQ2 −12V UNUSED +12V GND MEMW MEMR IOW IOR DACK3 DRQ3 DACK1 DRQ1 DACK0 CLK IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 DACK2 TC ALE +5V OSC GND GND MEMCS16 IRQ10 IRQ11 IRQ12 IRQ15 IRQ14 DRQ0 +5V MASTER

IOCHCK D7 D6 D5 D4 D3 D2 D1 D0 IOCHRDY AEN A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BHE D8 D9 D10 D11 D12 D13 D14 D15

BUS_EC1834_16Bit

+5V +12V −5V −12V GND

A0 AEN AENBRD AENBRDW AENDMA ALE BHE BS−/WAIT CLK CLK86 DACK0 DEN DT−/R DRQ0 DRQ1 DRQ2 DRQ3 HOLDA HRQDMA IED INT IOCHRDY IORW IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ8 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15 MASTER MDPEE MEMR NPAV NMI PB3 PCLK

Mario Gögel 2022
Sheet: /Bus/
File: Bus.kicad_sch

Title: EC1834 Hauptplatine 201.1−BUS

Size: A3	Date: 2022−09−12	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 6/6