AN3070
Application note

Managing the Driver Enable signal for RS-485 and IO-Link communications with the STM32™'s USART

Introduction

RS-485 and IO-Link are half-duplex communication protocols that offer easy ways of implementing the physical layer in industrial networks.

The STM32F10x, which comes with up to 5 UART interfaces and features fast DMA transfer and low interrupt latency, meets the RS-485 and IO-Link timing specifications.

This application note aims at providing timing measurements of the DE signal (Driver Enable) switching by using two different methods for managing this signal in RS-485 and IO-Link master transmission.

The application note is organized into three parts:

- it first explains why the timing of the DE signal is critical
- it then describes the two methods used to manage the DE signal
- and, finally, it gives different measurements of the DE signal switching time

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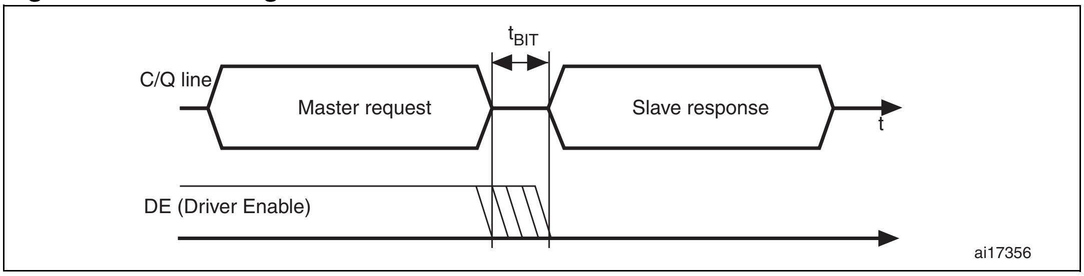
1 DE signal timing constraint

For serial half-duplex communication protocols like RS-485 & IO-Link, the master needs to generate a direction signal to control the transceiver (PHY). This signal informs the PHY if it must act in send or receive mode.

The timing of this control is critical, especially when switching from the send to the receive mode, as the application has to make sure that the device is in reception mode before data are sent by the other entity.

The master has to free the Tx/Rx line in no more than a bit time, otherwise there is a collision with the slave response. So the DE signal has to switch from high to low level within the bit time that follows the last bit of the last byte sent by the master.

Figure 1. DE timing constraint



The master should be able to guarantee the timing of the DE signal (imposed by the RS-485 & IO-Link specifications). The DE signal is managed by a GPIO.

Note that in this application note, the DE signal is emulated by GPIO port C pin 6 (PC6), however any GPIO could be used.

2 Description of the methods used to manage the DE signal

The purpose of this section is to provide two methods to control the DE signal and switch between the USART send and receive modes.

The first method uses two interrupts: the transmit complete interrupt of the DMA and the transmit complete interrupt of the USART.

The second method uses two USART interrupts: the transmit complete interrupt and the transmit buffer empty interrupt.

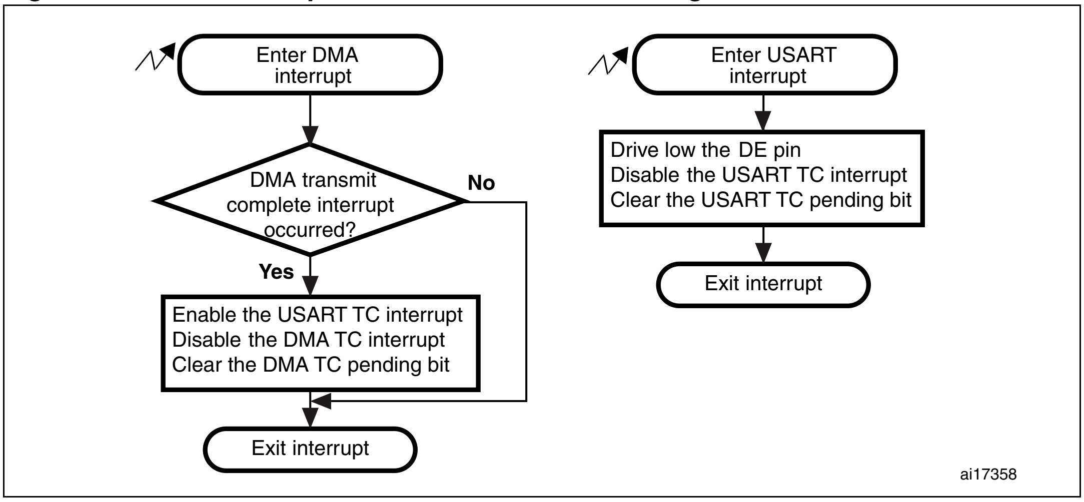
2.1 Method using the DMA interrupt

In this method, the DMA manages the data buffer transmission entirely. It continuously sends the data buffer to the USART data register until the DMA counter reaches 0. When the DMA transmit complete interrupt occurs, the USART transmit complete interrupt is enabled. In this interrupt, the DE pin is driven low.

The DE signal goes high just before the DMA transfer is enabled.

Figure 2 shows an example of management of the DE signal by using the DMA transmit complete interrupt.

Figure 2. DMA interrupt method to control the DE signal



2.2 Method using the USART interrupt

The transmit complete interrupt of the USART is used to drive low the DE pin, and so inform the slave to send its response. The transmit data register empty interrupt is also used to drive this pin high to inform that the master is to send data to the slave. *Figure 3* shows an example of the DE signal management using the USART interrupts.

The DE pin is pulled high before the first byte is sent. It is driven low after the last bit of the last byte is sent. This is done by enabling the TC interrupt during the last byte transmission. The next occurrence of the transmit complete interrupt drives the DE pin low.

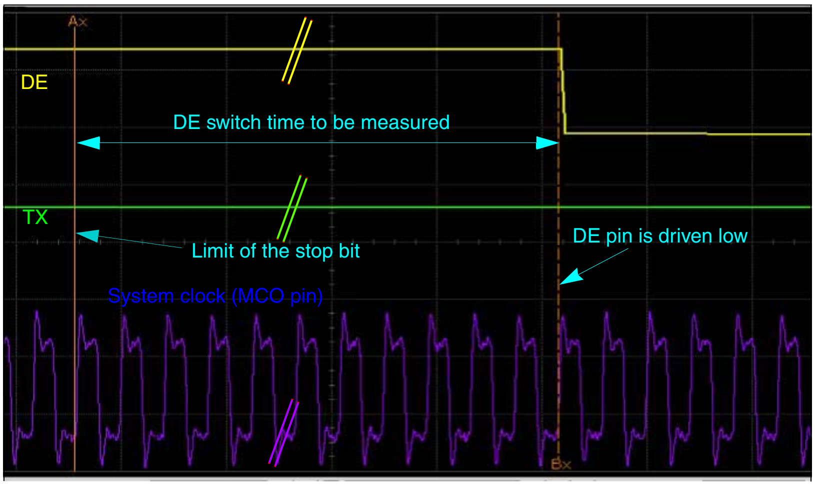
Figure 3. USART interrupt method to control the DE signal

3 Measuring the DE signal switching time using the two methods

This section gives some DE timing measurements using the two previously described methods.

The timing to be measured is the time interval between the end of the stop bit of the last byte and the falling edge of the DE signal. It is measured in CPU clock cycles (refer to *Figure 4*).

Figure 4. Zoom in DE signal switching period



The MCO pin (PA8) is used to output the system clock (CPU clock) in order to measure in CPU cycles the time taken by the DE signal to switch to the low level.

The end of the stop bit is evaluated by measuring the number of CPU clock cycles during a bit time.

This application note is released with two examples of firmware that implement the two previously described methods. Both examples describe the same sequence: drive PC6 high (DE signal), send a buffer of 4 bytes and then drive PC6 low.

The user can select the CPU frequency (72 MHz or 24 MHz) by commenting/uncommenting the following `define` in the *main.c* files:

```
#define HCLK_FREQ_72MHz
```

72 MHz is selected by default.

3.1 Measuring the DE signal switching time

This timing depends on different factors such as the compiler used, the level of optimization or the CPU frequency.

The examples are built with two compilers: Keil™ 4.00 and IAR 5.40.
They implement two optimization modes: low optimization and high optimization on timing.
The baud rate for transmission is 230400 baud (bit time = 4.34 µs), 1 stop bit.

3.1.1 Measuring the DE signal switching time using the DMA interrupt method

Table 1 gives the different timings measured at 72 MHz using the DMA interrupt method.

Table 1. Timing measurements of DE switching at 72 MHz

Compiler	Number of CPU cycles
IAR 5.40 / Keil 4.0	about 25

Table 2 gives the different timings measured at 24 MHz using the DMA interrupt method.

Table 2. Timing measurements of DE switching at 24 MHz

Compiler	Number of CPU cycles
IAR 5.40 / Keil 4.0	about 22

3.1.2 Measuring the DE signal switching time using the USART interrupt method

Table 3 gives the different timings measured at 72 MHz using the USART interrupt method.

Table 3. Timing measurements of DE switching at 72 MHz

Compiler	Number of CPU cycles
IAR 5.40 / Keil 4.0	about 43

Table 4 gives the different timings measured at 24 MHz using the USART interrupt method.

Table 4. Timing measurements of DE switching at 24 MHz

Compiler	Number of CPU cycles
IAR 5.40 / Keil 4.0	about 33

4 Conclusion

This application note presents two methods for managing the DE signal and guaranteeing the timing imposed by the RS-485 & IO-link specifications:

- The first method uses the DMA transmit complete interrupt and the USART transmit complete interrupt. It is easy to implement, and it leaves the CPU free to perform other tasks.
- The second method uses the USART interrupt. It does not require the DMA channel and so, can be implemented while the DMA is not available becaused used for other purposes.

Compared to the USART interrupt method, the DMA interrupt method achieves lower DE signal switching times. So, if DMA is available for data transmission, it is preferable to use it.

The two methods meet the RS-485 & IO-link timing requirement of 230 kbs transfer speed (bit time = 4.34 µs).

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Jan-2010	1	Initial release.