Using STM32 device PWM shut-down features
for motor control and digital power conversion

Introduction

The purpose of this application note is to describe the STM32 device timer break feature and show how it can be used with the other STM32 internal resources for an over-current and over-voltage protection in applications such as the motor control and the digital power conversion (lighting, SMPS, induction heating).

This application note:

- Provides an overview of the timer break feature,

- Details how the timer break input is connected to different break sources,

- Enumerates the different break event sources,

- Provides some scenarios of the PWM output signal response to break events coming from an internal source, an external source or a combination of both internal and external break signals,

- Shows how to implement over-current and over-voltage protections using the timer break feature and other embedded peripherals (such as comparators, DAC and so on).

This application note applies to the products listed in *Table 1*.

Table 1. Applicable products

Type	Product series
Microcontrollers	STM32F0 Series, STM32F1 Series, STM32F2 Series, STM32F3 Series, STM32F4 Series, STM32F7 Series, STM32L4 Series

Contents

List of tables

List of figures

1 Break function overview

The break function is available in TIM1, TIM8, TIM20, TIM15, TIM16 and TIM17 timers. These timers are able to generate complementary PWM signals with a dead time insertion for driving power switches in a half bridge topology.

The purpose of the break function is to protect power switches driven by PWM signals generated with these timers. When triggered by a fault, the break circuitry shuts down the PWM outputs and forces them to a predefined safe state.

Table 2 summarizes the break inputs availability.

Table 2. Timers and break input availability in STM32 devices

	TIM1	TIM8	TIM20	TIM15	TIM16	TIM17
STM32F0	BRK	-	-	-	-	-
	BRK_ACTH					
STM32F1	BRK	-	-	BRK	BRK	BRK
	BRK_ACTH			BRK_ACTH	BRK_ACTH	BRK_ACTH
STM32F2	BRK	BRK	-	-	-	-
	BRK_ACTH	BRK_ACTH				
STM32F3	BRK	BRK	BRK	BRK	BRK	BRK
	BRK2	BRK2	BRK2	BRK_ACTH	BRK_ACTH	BRK_ACTH
	BRK_ACTH	BRK_ACTH	BRK_ACTH	-	-	-
STM32F4	BRK	BRK	-	-	-	-
	BRK_ACTH	BRK_ACTH				
STM32F7	BRK	BRK	-	-	-	-
	BRK2	BRK2				
	BRK_ACTH	BRK_ACTH				
STM32L4	BRK	BRK	-	BRK	BRK	BRK
	BRK2	BRK2		BRK_ACTH	BRK_ACTH	BRK_ACTH
	BRK_ACTH	BRK_ACTH		-	-	-

The BRK input can either disable the PWM outputs (inactive state) or forces them to a predefined safe state, either active or inactive, after a dead time insertion which allows to prevent any shoot-through in the half bridge. The BRK2 only disables the PWM outputs (inactive state).

BRK has higher priority than BRK2. When both protections are triggered, the predefined safe state related to BRK circuitry overrides the inactive state related to the BRK2 input.

Typically, a permanent magnet 3-phase brushless motor drive will use the protections as follows:

- The BRK2 input as an over-current protection, opening the 6 switches from the power stage,

- The BRK input as an over-voltage protection, overriding the over-current and closing the 3 low-side switches to avoid current regeneration to build up the bus voltage and exceed the capacitor rated voltage.

As an example in the STM32F303xB/C/D/E devices, for a dual motor drive, the comparators 1, 2 and 3 can be affected to over-current monitoring of the 3 phases of motor 1 (BRK2 input of TIM1). The comparators 4, 5 and 6 can be affected to over-current monitoring of the 3 phases of motor 2 (BRK2 input of TIM8), while the comparator 7 will be used for over-voltage monitoring (driving BRK inputs of both TIM1 and TIM8).

BRK_ACTH input is connected only to internal signals like CSS, PVD output and so on. For more details, refer to *Section 2: Break implementation*.

The availability of break inputs and the break sources depends on the selected STM32 family. This is summarized in *Table 3*.

Table 3. Peripherals availability per STM32 devices

	STM32F0		STM32F1		STM32F2	STM32F3							STM32F4		STM32F7	STM32L4
	STM32F05xxx / STM32F07xxx / STM32F09xxx	STM32F03xxx	STM32F100xx	STM32F101xx / STM32F102xx / STM32F103xx / STM32F105xx / STM32F107xx	STM32F205xx / STM32F207xx / STM32F215xx / STM32F217xx	STM32F303xB/C / STM32F358xC	STM32F303x6/8 / STM32F328x8	STM32F303xD/E / STM32F398xE	STM32F302xB/C/D/E	STM32F302x6/8 / STM32F301x6/8 / STM32F318x8	STM32F334x4/6/8	STM32F37xxx	STM32F401B/Cx / STM32F401D/Ex / STM32F410xx / STM32F411xC/E	STM32F4x5xx / STM32F4x7xx / STM32F4x9xx / STM32F446xx	STM32F75xxx / STM32F74xxx	STM32L4x6xx
DFSDM	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X
COMP1	X	-	-	-	-	X	-	X	X	-	-	X	-	-	-	X
COMP2	X	-	-	-	-	X	X	X	X	X	X	X	-	-	-	X
COMP3	-	-	-	-	-	X	-	X	-	-	-	-	-	-	-	-
COMP4	-	-	-	-	-	X	X	X	X	X	X	-	-	-	-	-
COMP5	-	-	-	-	-	X	-	X	-	-	-	-	-	-	-	-
COMP6	-	-	-	-	-	X	X	X	X	X	X	-	-	-	-	-
COMP7	-	-	-	-	-	X	-	X	-	-	-	-	-	-	-	-
TIM1	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X	X
TIM8	-	-	-	X	X	X	-	X	-	-	-	-	-	X	X	X
TIM15	X		X	-	-	X	X	X	X	X	X	X	-	-	-	X
TIM16	X	X	X	-	-	X	X	X	X	X	X	X	-	-	-	X
TIM17	X	X	X	-	-	X	X	X	X	X	X	X	-	-	-	X
TIM20	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-	-

2 Break implementation

2.1 TIM1/8/20 break implementation

The source for break BRK channel is an external source connected to one of the BKIN pin (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source of break2 BRK2 channel is an external source connected to one of the BKIN2 pin (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source for BRK_ACTH is an internal signal coming from:

– Comparator output.
– Clock Security System
– Cortex M4 lockup
– PVD Output
– SRAM Parity error signal
– Flash ECC error

Note: *In STM32L4 Series, the comparators output are connected to the BRK and the BRK2 (no connection to the BRK_ACTH)*

BRK

– In STM32F0/F1/F2/F4/F7 series: The input signal on BRK is connected to the BKIN pin.
– In STM32F3 Series: The input signal on BRK is a logical OR between the input signals on BKIN pin and the used comparator (4 or 7) output if configured and used internally. If BKIN alternate function is disabled, the resulting break signal is the comparator (4 or 7) output.
– In STM32L4 Series: The input signal on BRK is a logical OR between the input signals on BKIN pin, the used comparator (1 or 2) output and the DFSDM break output if configured and used internally. Each application break source has its own polarity configuration.

When the BRK input is used, the polarity feature is available. The filter feature is available as well but only on STM32F3/F7/L4 devices.

BRK_ATCH

– In STM32F1/F2/F4/F7 series: this input only gathers the system level fault signals.
– In STM32F0 Series: BRK_ACTH is connected to the system level fault signals and the Comparators outputs (1 and 2).
– In STM32F3 Series: BRK_ACTH is connected to the system level fault signals and the comparators (1, 2, 3, 5 and 6).
– In STM32L4 Series: BRK_ACTH is connected to the system level fault signals and the digital filter for sigma delta modulators output (DFSDM).

When this input is used, the polarity selection and filter features are not available. It is always active high.

BRK_ACTH is enabled using the same bit as BRK (BKE in TIMx_BDTR, x= 1, 8, 20).

When using BRK_ACTH as break input, the polarity must be configured High. Otherwise, there will be no PWM generation independently of the break signal coming from the internal source.

If there are several break input sources, the resulting input signal will be an OR between all the input signals.

In the particular case where there is an internal break input signal connected to BRK_ACTH and an external input signal coming through the BKIN pin (BKIN alternate function is enabled), the resulting break input signal will be an OR between the signal on BKIN and the internal break signal.

BRK2

–   In STM32F3 Series: this input signal is a logical OR between the input signal on BKIN2 pin and the used comparators outputs (1, 2, 3, 4, 5, 6 and 7). If BKIN2 alternate function is disabled (input not used), the resulting break signal is solely related to the comparators.

–   In STM32F7 Series: the input signal on BRK2 is connected to the BKIN2 pin.

–   In STM32L4 Series: the input signal on BRK2 is a logical OR between the input signals on BKIN2 pin, the used comparator (1 or 2) output and the DFSDM break output if configured.

In STM32L4 Series, it is possible to configure the polarity of each break source in addition except the DFSDM break output to the polarity configuration inside the timer peripheral using BKCMP1P, BKCMP2P, BKINP in TIMx_OR2 register and BK2CMP1P, BK2CMP2P, BK2INP in TIMx_OR3 register.

The polarity selection and filter features are available when BRK2 is used.

Figure 1 shows the break feature implementation for TIM1, TIM8 in STM32F0/F1/F2/F4/F7 Series devices.

Figure 2 shows the break feature implementation for TIM1, TIM8 and TIM20 in STM32F3 Series devices.

Figure 3 shows the break feature implementation for TIM1 and TIM8 in STM32L4 Series devices.

Figure 1. Break feature implementation in advanced timers for STM32F0/F1/F2/F4/F7 Series devices
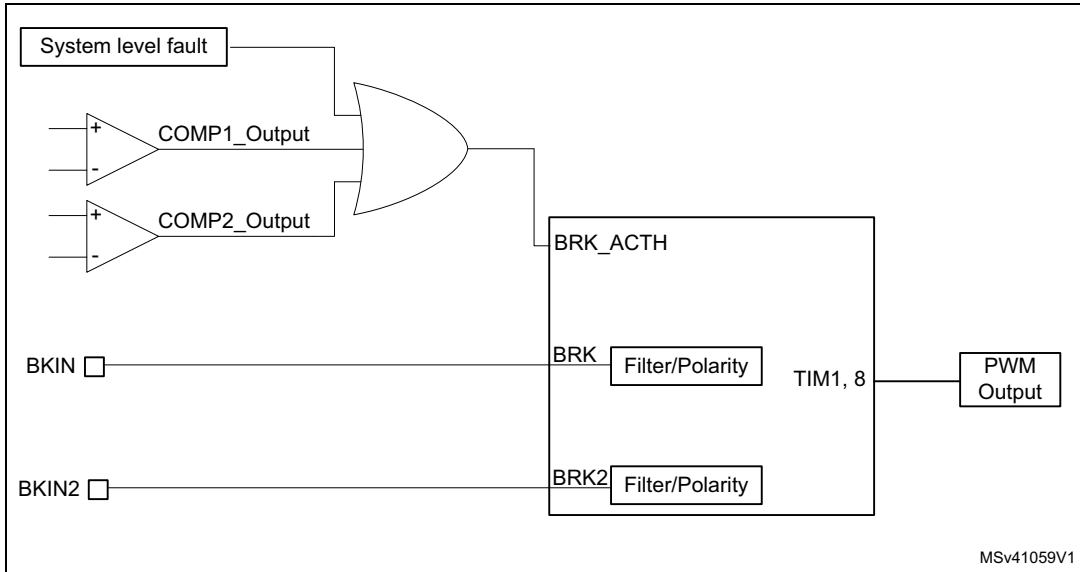
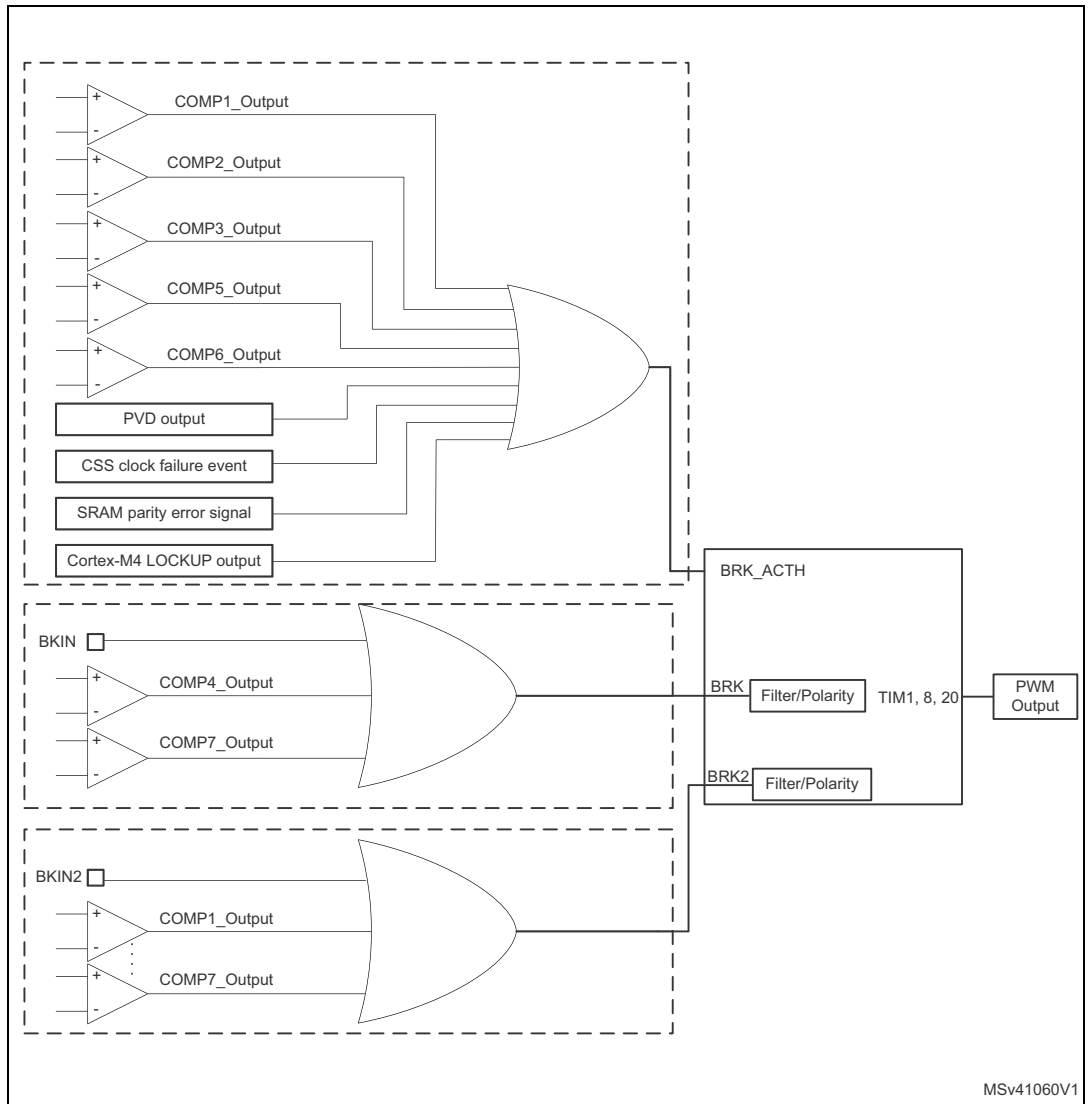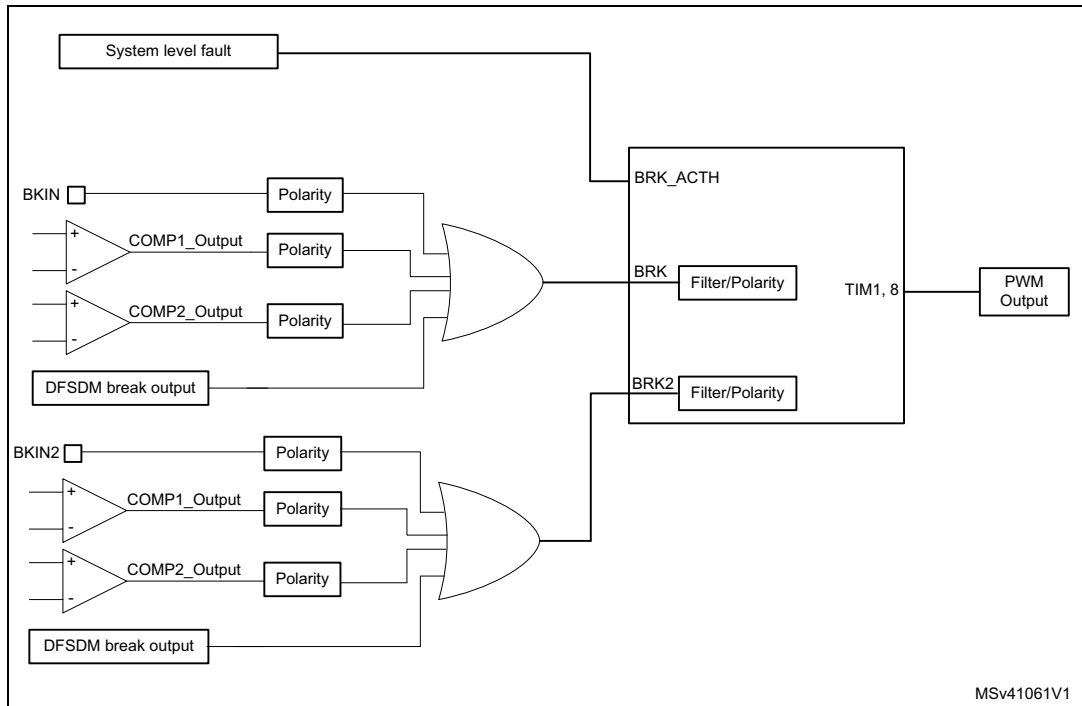**Figure 2. Break feature implementation in advanced timers for STM32F3 Series devices**

MSv41060V1

Figure 3. Break feature implementation in advanced timers for STM32L4 Series devices

**Bidirectional break inputs**

Only in STM32L4 Series, the timer 1 and timer 8 are featuring bidirectional break input/outputs combining the comparator output (to be configured in open drain) and the Timer BKIN input, as represented in *Figure 4*.

This feature allows to have the information about the global break available for external MCUs with a single-pin.

Figure 4. Output redirection
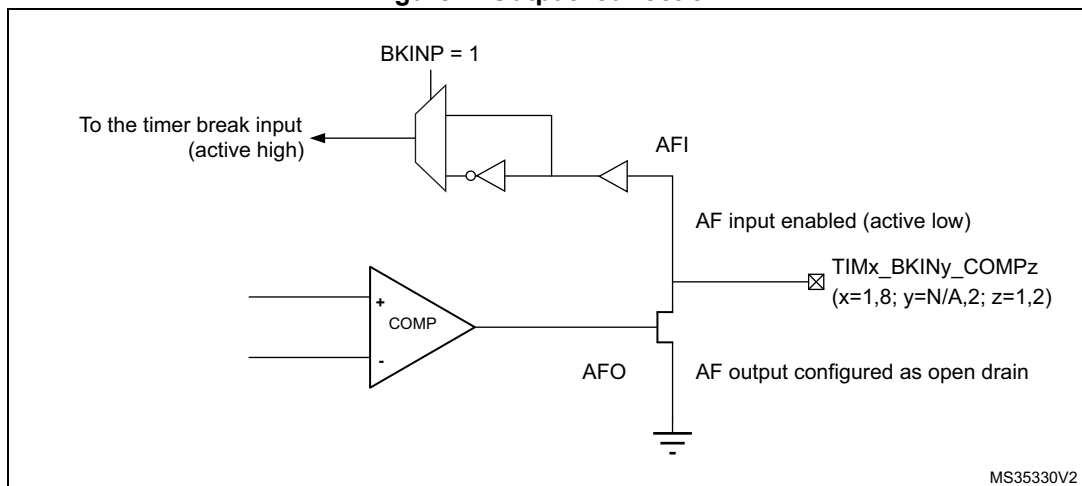
2.2 TIM15/16/17 break implementation

The source for break BRK channel is an external source connected to one of the BKIN pin (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source for BRK_ACTH is an internal signal coming from:

- – Comparator output.
- – Clock Security System
- – Cortex M4 lockup
- – PVD Output
- – SRAM Parity error signal
- – Flash ECC error

Note: *In STM32L4 Series, the comparators output are connected to the BRK (no connection to the BRK_ACTH).*

BRK

- – In STM32F0/F1/F2/F3/F4/F7 series: the input signal on BRK is connected to the BKIN pin.
- – In STM32L4 Series: the input signal on BRK is a logical OR between the input signals on BKIN pin, the used comparator (1 or 2) output and the DFSDM break output if configured.

The polarity selection feature is available when BRK is used.

In STM32L4 Series, it is possible to configure the polarity of each break source in addition except the DFSDM break output to the polarity configuration inside the timer peripheral using BKCMP1P, BKCMP2P, BKINP in TIMx_OR2 register.

Note: *The filter feature is available only in STM32L4 Series.*

BRK_ACTH

- – In STM32F1/L4 Series: This input only gathers the system level fault signals (CSS, PVD output, SRAM parity error and the Hardfault).
- – In STM32F3 Series: BRK_ACTH is connected to the system level fault signals and the comparators (1 and 2) for the STM32F37xxx devices and the comparators outputs (3, 5 and 7) for the rest of STM32F3 Series.

When this input is used, the polarity selection and filter features are not available. It is always active high.

BRK_ACTH is enabled using the same bit BRK (BKE in TIMx_BDTR, x= 15, 16, 17).

When using BRK_ACTH as break input, the polarity must be configured High. Otherwise, there will be no PWM generation independently of the break signal coming from the internal source.

Figure 5 shows the break feature implementation for TIM15, TIM16 and TIM17 in STM32F1 Series devices.

Figure 6 shows the break feature implementation for TIM15, TIM16 and TIM17 in STM32F3 Series devices.

Figure 7 shows the break feature implementation for TIM15, TIM16 and TIM17 in STM32L4 Series devices.

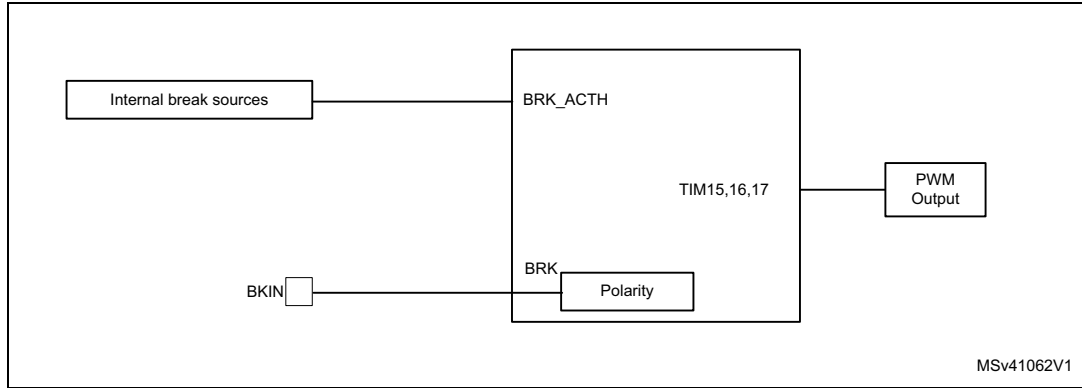**Figure 5. Break feature implementation for TIM15, TIM16 and TIM17 for STM32F1 Series devices**

Figure 6. Break feature implementation for TIM15, TIM16 and TIM17 for STM32F3 Series devices
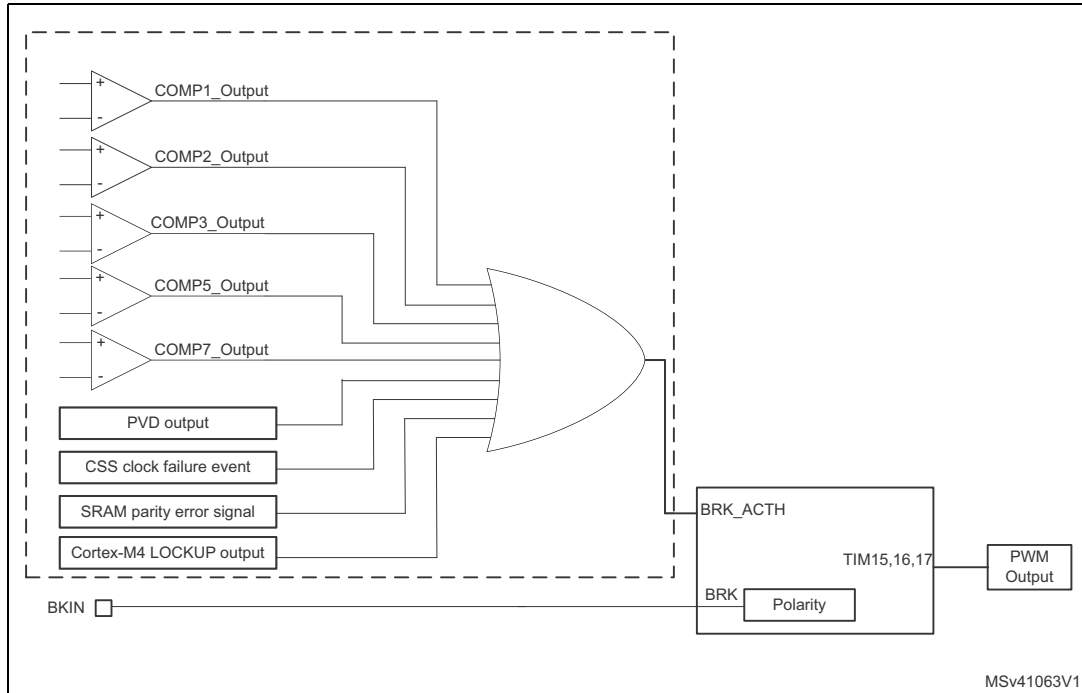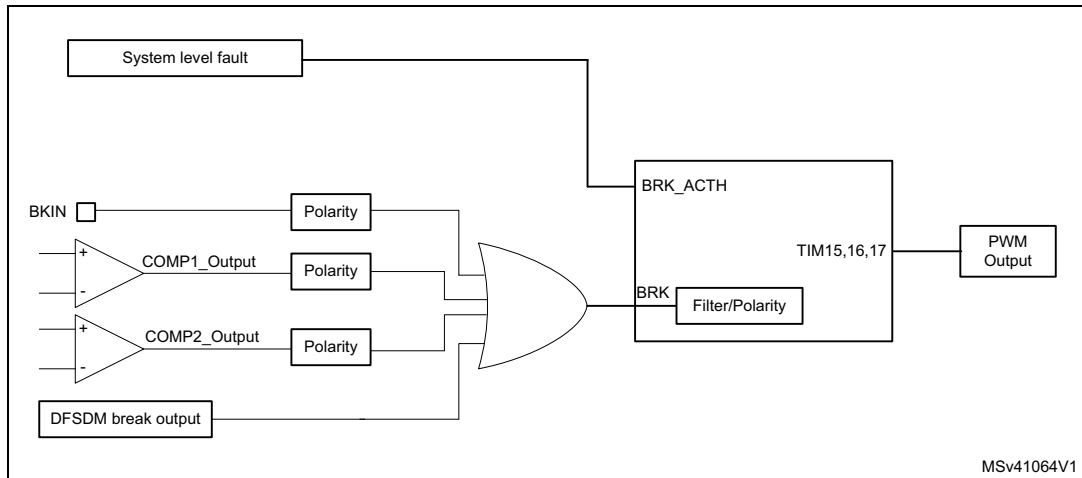
Figure 7. Break feature implementation for TIM15, TIM16 and TIM17 for STM32L4 Series devices

- If only an internal break source is used, the polarity must be configured to "High" in the software.
- If there are several break input sources, the resulting input signal will be an OR between all the input signals.
- If both internal break source and BKIN are used, the resulting break signal will be an OR between the signal pin and the internal break signal.
- If the Alternate function AF of the BKIN or BKIN2 pin is not activated, the BRK or the BRK2 will be connected to the ground, and if the state of the BRK or BRK2 polarity is "Low", in this case if the break function is enabled, the timer output will be disabled. So it must to configure the break polarity to "High". Only in STM32F1 Series it must to configure the break polarity to "Low".

3 Break sources summary

Table 4 summarizes the available break sources and their connections externally or internally to timers (1, 8, 20, 15, 16, and 17) break inputs.

Table 4. Break input sources

	BRK	BRK_ACTH	BRK2
External connection to pin	BKIN	No corresponding I/O	BKIN2
Internal connection to	**In STM32F3:** - Comparators 4 and 7 for TIM1/8/20 - NA for TIM15/16/17 **In STM32L4:** - Comparators 1 and 2 for TIM 1/8/15/16/17 - DFSDM break output	- Clock failure event generated by CSS - PVD output - RAM parity error signal - Cortex-M4 LOCKUP output (Hardfault) - Comparator outputs	**In STM32F3:** - Comparators 1, 2, 3, 4, 5, 6 and 7 **In STM32L4:** - Comparators 1 and 2 - DFSDM break output.
Polarity feature in case of internal connection	Configurable: active high or active low	Always active high	Configurable: active high or active low
Filter feature in case of internal connection	Available in STM32L4 and available in STM32F3 only for advanced timers	Filter feature is NOT available	Available only in STM32F3 and STM32L4
Polarity feature in case of external break event	Available	NA	Available
Filter feature in case of external break event	Available in STM32F3, STM32F7 and STM32L4	NA	Available only in STM32F3, STM32F7 and STM32L4
Available in	TIM1/8/20/15/16/17	TIM1/8/20/15/16/17	TIM1/8/20 in STM32F3, STM32F7 and STM32L4
Resulting break signal in case of parallel external or/and internal break sources	It is an OR between the external break signal(s) and the internal one(s)		

4 Examples

Table 5 shows the PWM output status for TIMx (where x= 1, 8, 20, 15, 16, 17) in response to internal/external break events.

In the following waveforms:

- "PWM" signal is the reference waveform (internal signal, before BRK protection).
- "COMP_OUT" signal represents the BRK input signal, in our case it is the comparator output.
- "BIN" signal is the input signal on BKIN.
- "PWM_BRK" signal is the resulting PWM signal on the timer output after break detection.

Color legend for Table 5: green = PWM signal, blue = COMP_OUT signal, yellow = BKIN signal, purple = PWM_BRK signal.

Table 5. Scenarios of PWM output status in response to internal/external break events
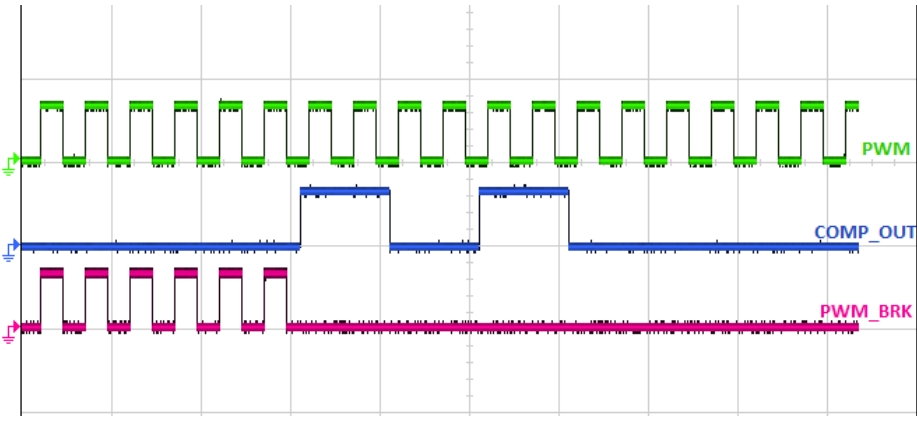
Configuration	Programmed polarity	Result
Comparator 1 output is connected internally to TIM1 BRK_ACTH and TIM1 BKIN alternate function is disabled.	High	The PWM generation is stopped when the comparator output is at the high level, as shown in the following screen shot:

Table 5. Scenarios of PWM output status in response to internal/external break events (continued)
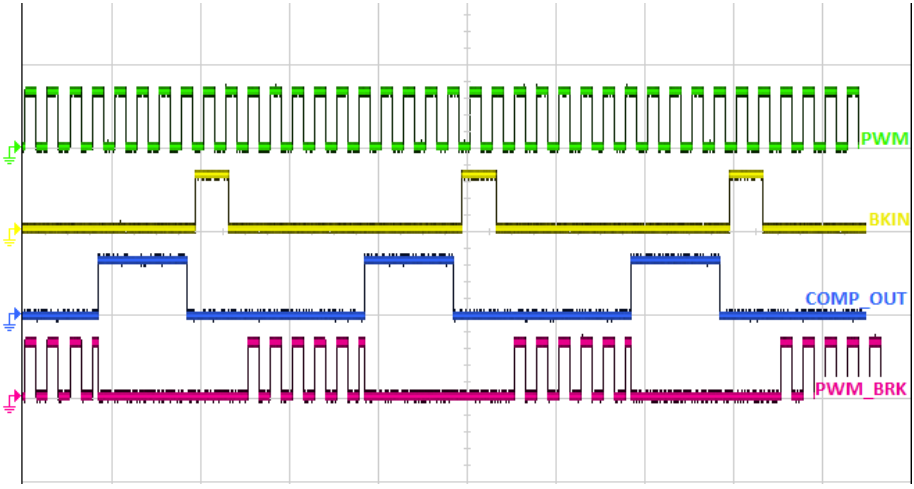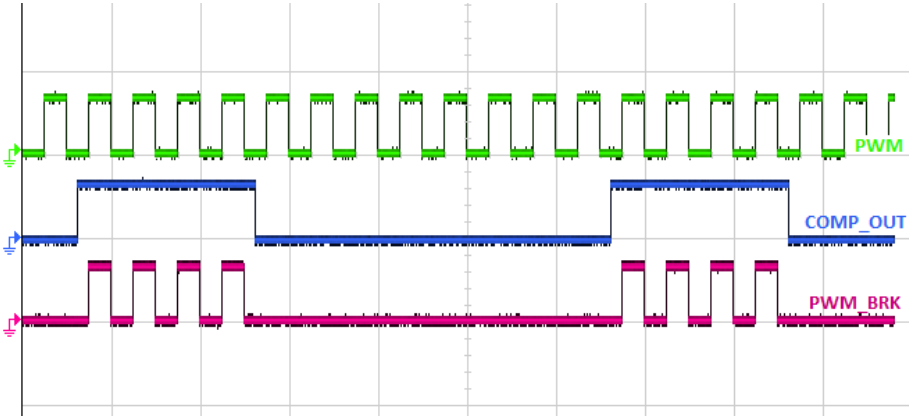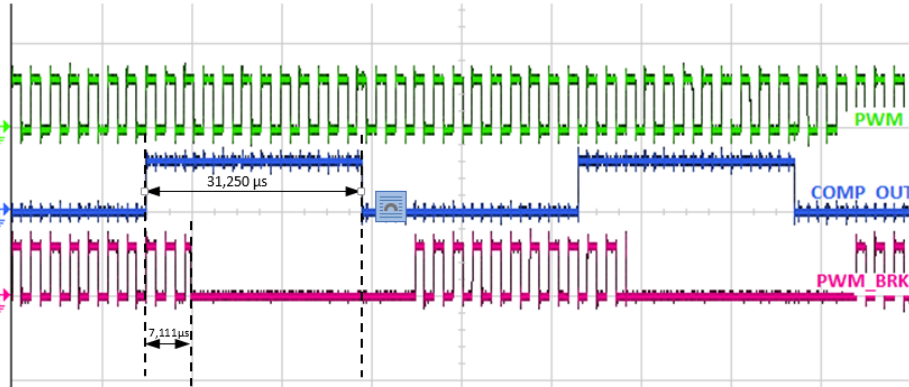
Configuration	Progra- mmed polarity	Result
Comparator 1 output is connected internally to TIM1 BRK_ACTH and TIM1 BKIN alternate function is enabled.	High/ Low	The break input signal is an OR between the signal on BKIN and the comparator output. The following screen shot shows an example (polarity = High): *Note:* *In order to show the effect of the two break sources, the bit AOE in BDTR register is set, allowing to re-start the PWM at the next update event.*

Table 5. Scenarios of PWM output status in response to internal/external break events (continued)

| Configuration	Progra-mmed polarity	Result
Comparator 4 output is connected internally to TIM1 BRK and filter is not configured.	Low	The PWM signal is stopped during the break signal low level, as shown in the following screen shot:
Comparator 4 output is connected internally to TIM1 BRK and filter is configured.	High	During the window defined by the filter duration, the break event has no impact on the PWM generation even if the break condition is verified. This is the case of the following example (screen shot) where the PWM signal is generated normally when the break signal is at high level during the window defined by the filter. – The filter duration is 7.111 µs (BKF = 1111b, filter duration is (32*8/fDTS), fDTS = 36 MHz). – The comparator output high level duration is 7.111 µs.

5 Using the break function with other MCU resources

Note: *This section is dealing with the STM32F3 Series, but some parts are also applicable for other STM32 series.*

5.1 Break function used for over-current protection

The STM32F3 Series microcontroller embeds a set of peripherals designed to resolve common motor control issues by reducing the number of required external components. This section describes how to use these peripherals to implement over-current protection. *Figure 8* shows the over-current protection network that can be implemented using the internal resources of the STM32F3 Series.

Figure 8. Over-current protection network implemented with STM32F3 Series devices
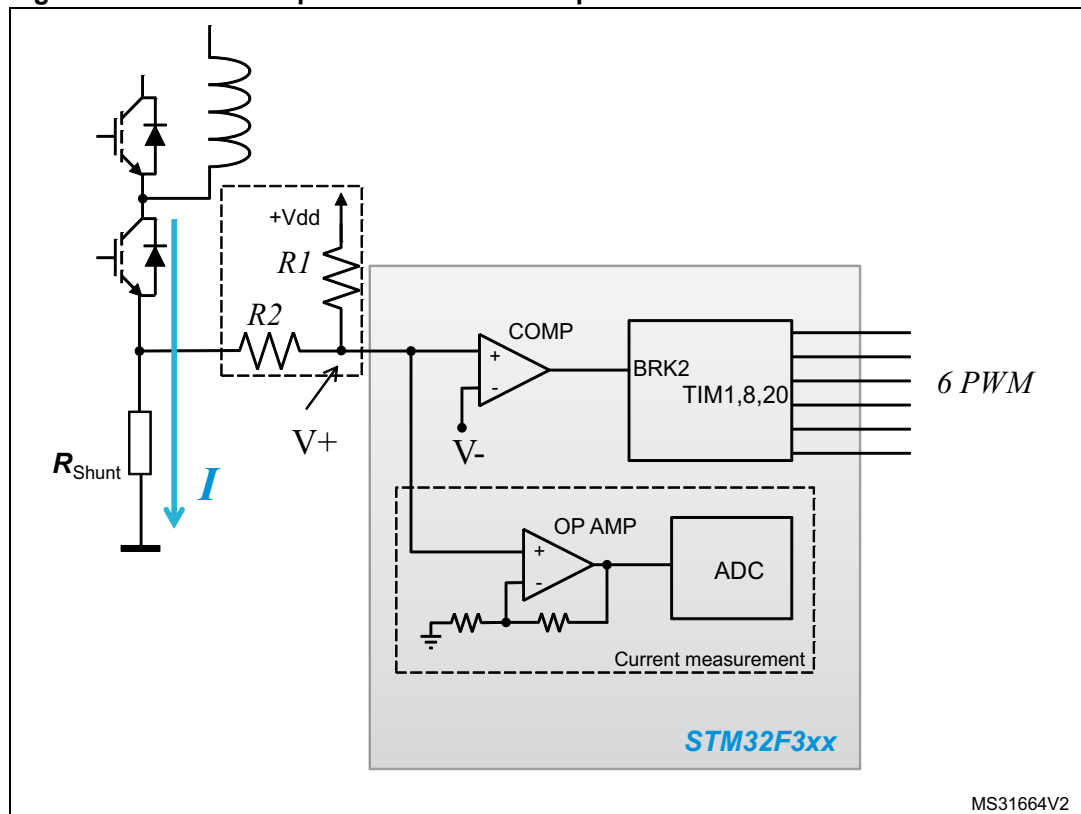
The principle of this over-current protection mechanism can be summarized as follows:

- The phase current of the motor flows in the power transistor of the inverter bridge and passes through the shunt resistor (R_{Shunt}) producing a voltage drop (V+).
- This voltage drop is compared with a threshold (V-) defining the maximum admissible current.
- If the threshold is exceeded, a break signal stops the PWM generation putting the system in a safe state.

All of these actions can be performed using the internal resources of the STM32F3 Series and, in particular, the embedded comparators and advanced timer break function (BRK2). In

the basic implementation, the only external component required is the shunt resistor that must be sized depending on the current to be monitored and the shunt resistor power rating.

The two dotted line boxes in *Figure 8* show the components required to measure current:

- The R1/R2 resistive network to add an offset necessary to measure AC currents.
- An operational amplifier with a built-in gain setting network.

The amplification network can be implemented externally for specific use cases where the built-in gain settings are not adequate.

5.2 Break function used for over-voltage protection

Figure 9 shows the over-voltage protection network that can be implemented using the internal resources of the STM32F3 Series.

Figure 9. Over-voltage protection network implemented with STM32F3 Series devices
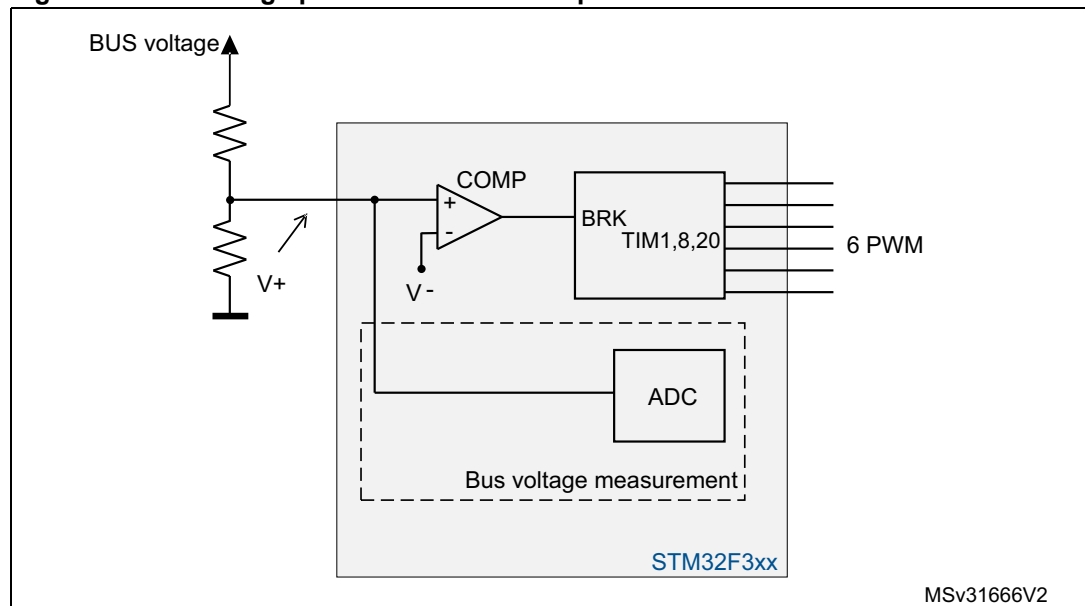
In this case, the principle is similar to the one described in *Section 5.1*:

- A resistive voltage divider provides a signal proportional to the bus voltage.
- This reading is compared to an over-voltage threshold to generate a fault signal. See also: *Appendix A: How to use the DAC to define thresholds*.
- If the threshold is exceeded, a break signal stops the PWM generation putting the system in a safe state.

As mentioned before, these actions can be performed automatically using the internal comparator of the STM32F3 Series. In this case, it is possible to use the second break functionality (BRK) of the advanced timer in order to differentiate the action to perform on the PWM signals in case of an over-current.

In the basic implementation, the only external component required is the voltage divider which must be sized depending on the bus voltage range requested by the target application, so that it never exceeds the MCU's input maximum admissible voltage level.

The dotted line box in *Figure 9* shows the components required for the bus voltage measurement. In this case, amplifying the signal V+ is usually not required (the resistive divider is adjusted for full-range reading), so this signal is fed directly to the analog-to-digital converter.

5.3 Using an external emergency signal together with the internal comparator

Commonly in MC applications, gate driver ICs - such as ST's L639x family - or Intelligent Power Modules (IPMs) - such as ST's "SLLIMM" (Small Low-Loss Intelligent Molded Module) family - have integrated comparators that can protect the inverter (ST's "Smart Shutdown" function) while sending an error signal to the microcontroller.

In this section, we will see that it is possible to combine these two concepts, as shown in *Figure 10*, so as to enhance by redundancy the functional safety offered by the "break function".

A first option is when the break function is triggered by internal comparators output only: the error signal coming from ICs or IPMs should not be connected to the microcontroller, thus saving the pin. The configuration to be set in this case is summarized in the following table:

Table 6. Comparator output connected internally to break inputs

Description	Register	Bit	Configuration
TIM1/8/20 BRK_ACTH/BRK/BRK2 polarity	TIMx_BDTR	BKP or BK2P	1 (active high)
Comparator output polarity	COMPx_CSR	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN and BKIN2 AF	GPIOxAFRL or GPIOxAFRH	-	AF not enabled on BKIN1/2 related pins
TIM1/8/20 BRK and BRK2 enable	TIMX_BDTR	BKE or BK2E	1
COMPx out selection	COMPx_CSR	COMPxOUTSEL	0001: TIM1 BRK or TIM1 BRK_ACTH[1] 0010: TIM1 BRK2 0011: TIM8 BRK or TIM8 BRK_ACTH[2] 0100: TIM8 BRK2 0101: TIM1 BRK2 + TIM8 BRK2 1100: TIM20 BRK or TIM20 BRK_ACTH[3] 1101: TIM20 BRK2 1110: TIM1 BRK2 + TIM8 BRK2 + TIM20 BRK2

1. TIM1 BRK in case of COMP4 and COMP7, or TIM1 BRK_ACTH in case of COMPx, x = 1, 2, 3, 5 and 6.

2. TIM8 BRK in case of COMP4 and COMP7, or TIM8 BRK_ACTH in case of COMPx, x = 1, 2, 3, 5 and 6.

3. TIM20 BRK in case of COMP4 and COMP7, or TIM20 BRK_ACTH in case of COMPx, x= 1, 2, 3, 5 and 6.

On the contrary, the user may prefer to make use of the external error signal in conjunction with the internal one: the result is an OR between the two. Depending on the external comparator logic, the possible configurations to be written are summarized in the following tables:

Table 7. Comparator output connected externally to break inputs,
**with low break polarity**

Description	Register	Bit	Configuration
TIM1/8/20 BRK polarity	TIMx_BDTR	BKP	0 (active low), it means that the external signal goes low during the fault
Comparator output polarity	COMPx_CSR	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN AF	GPIOxAFRL or GPIOxAFRH	-	AF enabled on BKIN pin selected among available
TIM1/8/20 BRK enable	TIMX_BDTR	BKE	1
COMPx out selection	COMPx_CSR	COMPxOUTSEL	0001: TIM1 BRK 0011: TIM8 BRK 1100: TIM20 BRK

Table 8. Comparator output connected externally to break inputs,
with high break polarity

Description	Register	Bit	Configuration
TIM1/8/20 BRK/BRK2 polarity	TIMx_BDTR	BKP or BK2P	1 (active high), it means that the external signal goes high during the fault
Comparator output polarity	COMPx_CSR	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN/BKIN2 AF	GPIOxAFRL or GPIOxAFRH	-	AF enabled on BKIN/BKIN2 pin selected among available
TIM1/8/20 BRK/BRK2 enable	TIMX_BDTR	BKE or BK2E	1
COMPx out selection	COMPx_CSR	COMPxOUTSEL	0001: TIM1 BRK 0010: TIM1 BRK2 0011: TIM8 BRK 0100: TIM8 BRK2 0101: TIM1 BRK2 + TIM8 BRK2 1100: TIM20 BRK 1101: TIM20 BRK2 1110: TIM1 BRK2 + TIM8 BRK2 + TIM20 BRK2

The comparators output can be optionally enabled as alternate function on the related GPIO pin, in push-pull or open-drain mode, for signaling to other devices or for debugging purposes.

Figure 10. Combining external and internal protection concept
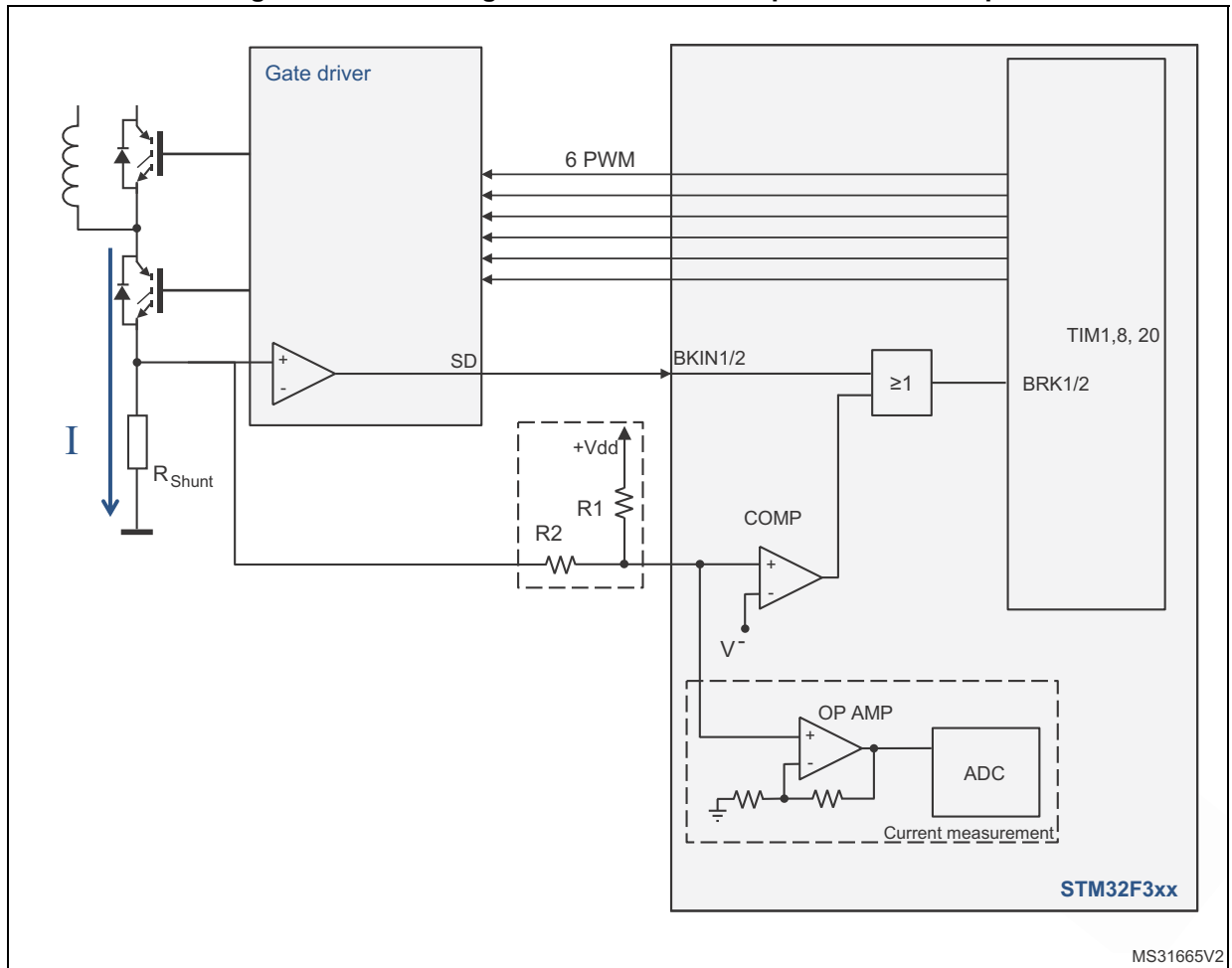
5.4 Filtering the break input

Programmable filters are available to prevent break functions of advanced timers from being triggered on spurious events (switching noise for instance).

The digital filter feature is available on BRK and BRK2. It is not available on BRK_ACTH.

That means that the digital filter is:

- Available when the break source is external and comes from the external inputs BKIN/BKIN2,
- Available when the break source is internal and connected to BRK or BRK2,
- Not available when the break source is internal and connected to BRK_ACTH.

5.5 Locking the selected configuration

Electrical motor drives require a high level of reliability and robustness for the potential damages that may be caused in case of failure.

To increase robustness against software runaways, the STM32F3 Series microcontroller comes with a chain of peripherals featuring the lock feature, beginning from the mode of the GPIO pins used for sensing through comparators, operational amplifiers (opamp) and advanced timers, down to the GPIO pins used for driving, as shown in *Figure 11*.

In particular, BRK and BRK2 configurations can be locked using the LOCK bits in TIMx_BDTR register. At least LOCK level 1 is recommended to freeze DTG/BKE/BKP/AOE/BKF/BK2F/BK2E/BK2P bits in TIMx_BDTR register and OISx/OISxN bits in TIMx_CR2 register until the next reset.

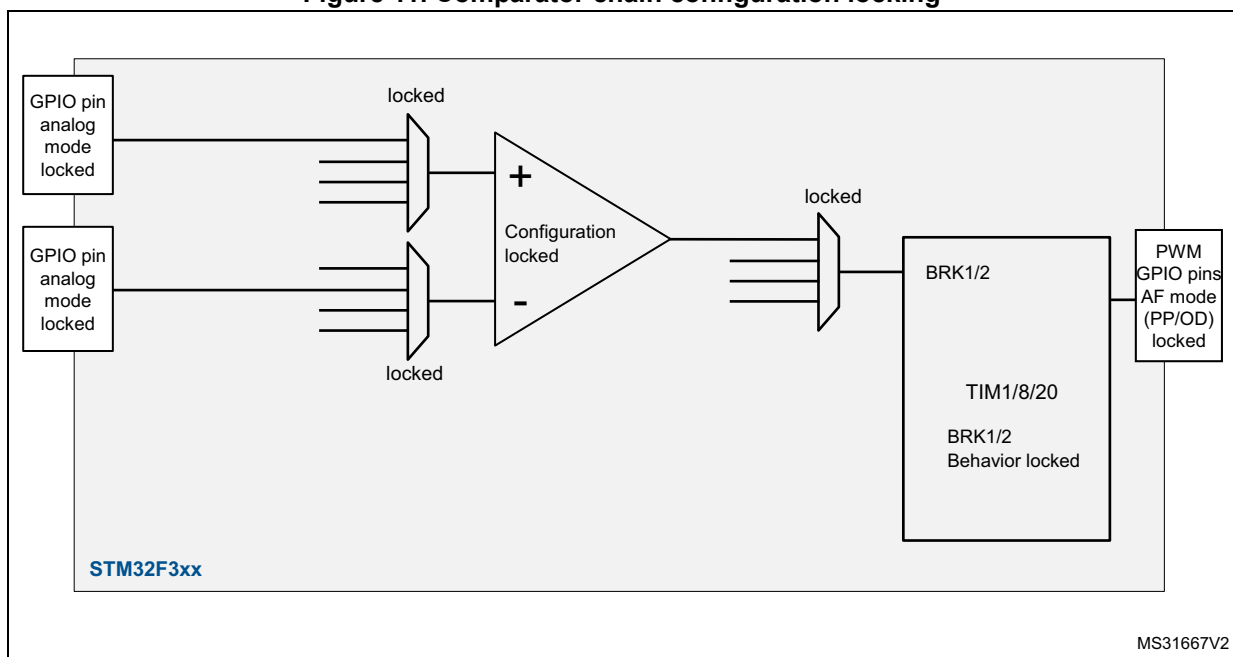**Figure 11. Comparator chain configuration locking**

Table 9 summarizes the recommended settings for comparators.

Table 9. Register locking mechanism

| Peripheral	Feature	Register	Comment
GPIO Port x, pin y	Inverting input, pin mode selection	GPIOx_MODER register, MODERy bit to be configured in "Analog mode"	-
GPIO Port x, pin y	Inverting input, pin configuration locking	GPIOx_LCKR register, specific write sequence coded with LCKy bit	MODERy bit (in GPIOx_MODER register) now frozen until next reset
GPIO Port w, pin z	Non inverting input, pin mode selection	GPIOw_MODER register, MODERz bit to be configured in "Analog mode"	Not needed if an internal reference is selected
GPIO Port w, pin z	Non inverting input, pin configuration locking	GPIOw_LCKR register, specific write sequence coded with LCKz bit	MODERz bit (in GPIOw_MODER register) now frozen until next reset
TIMER 1/8/20	BKIN / BKIN2 configuration locking	TIMx_BDTR register, LOCK bits	LOCK level 1 (at least) recommended: DTG bits in TIMx_BDTR register, OISx and OISxN bits in TIMx_CR2 register and BKE/BKP/AOE bits in TIMx_BDTR register frozen until next reset

Appendix A   How to use the DAC to define thresholds

Concerning the network shown in *Figure 8* and *Figure 9*, it is important to properly set the comparator inverting input voltage (V-) to define the threshold levels for over-current protection and over-voltage protection.

As shown in *Figure 12* below, in the STM32F3 Series microcontroller it is possible to set three different sources as inverting input for the comparator:

- An external reference (GPIO),
- A fixed internal reference (Vref, ¾ Vref, ½ Vref, ¼ Vref),
- A programmable internal reference (DAC).

Figure 12. Inverting input selection
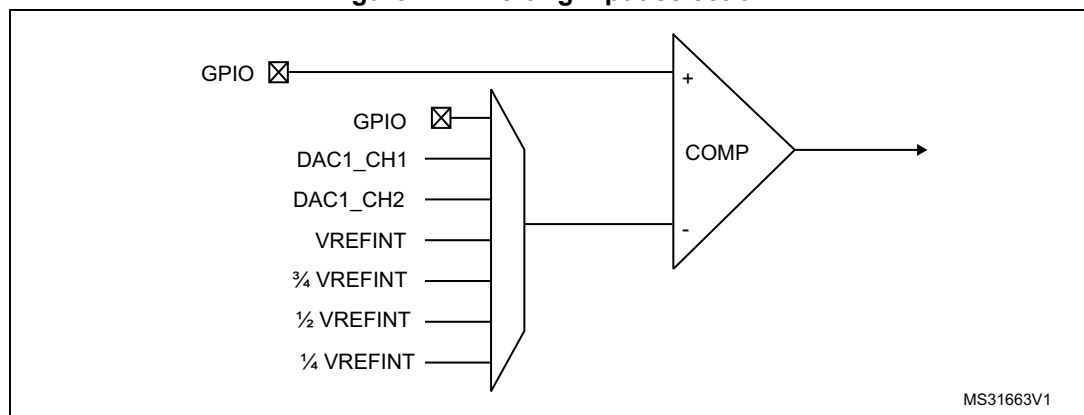
Practical example: Over-current protection using the offset network

This is the case of *Figure 8* when the components inside the dotted line boxes are present. In this case, the formula to compute the over-current threshold is the following:

Equation 1

$$I_{th} = \frac{V^- - \left(V_{dd} \times \dfrac{R_2}{R_1 + R_2}\right)}{R_{shunt} \times \left(\dfrac{R_1}{R_1 + R_2}\right)}$$

Usually the R_1 and R_2 values are used to satisfy the current measurement needs. It is clear that using the internal reference for V^- can lead to a threshold value I_{th} which is not exactly coincident with the required one. As explained in this practical example, the internal reference can be used only when there is no need to fine-tune the over-current threshold. Otherwise, it is necessary to use the external reference or the variable internal reference. The latter is recommended, because it does not require any external components.

The STM32F3 Series microcontroller includes two 12-bit DAC channels that can be used for this purpose. For three-phase motor drives, it is possible to group three comparators to protect each leg of the inverter bridge versus over-current by setting the same DAC channel for all three inverter inputs.

The same can be done in case of dual motor control with also having the possibility to define two different levels of protection, one for each motor.

Revision history

Table 10. Document revision history

Date	Revision	Changes
25-Nov-2013	1	Initial release.
05-Mar-2015	2	Updated cover page with STM32F3 Series and adding RM references. Updated the whole document adding TIM20 and replacing STM32F30x/31 x by STM32F3 Series. Updated *Section 1: Break function overview* adding *Table 3: Peripherals availability per STM32 devices*. Updated *Figure 1: Break feature implementation for TIM1, TIM8 and TIM20*. Updated *Figure 11: Comparator chain configuration locking*. Updated *Table 9: Register locking mechanism*.
30-Jun-2015	3	Updated *Section 2.2: TIM15/16/17 break implementation* removing the filter feature in BRK and BRK_ACTH paragraphs. Updated *Figure 5: Break feature implementation for TIM15, TIM16 and TIM17 for STM32F1 Series devices* replacing filter/polarity by polarity. Updated *Table 4: Break input sources* adding "NA for TIM15/16/17" for 2 lines in BRK column.
03-May-2016	4	Updated cover page title and introduction with the application note applying to STM32 devices. Added *Table 1: Applicable products*. Updated *Section 1: Break function overview*. Added *Table 2: Timers and break input availability in STM32 devices*. Updated *Table 3: Peripherals availability per STM32 devices*. Updated *Section 2: Break implementation*. Updated *Figure 1*, *Figure 2*, *Figure 3*, *Figure 5*, *Figure 6* and *Figure 7*. Updated *Table 4: Break input sources*. Updated *Table 5: Scenarios of PWM output status in response to internal/external break events*. Updated *Section 5: Using the break function with other MCU resources* adding a note. Updated *Section : BRK_ATCH*. Added *Section : Bidirectional break inputs*. Added *Figure 4: Output redirection*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY